SECTION 10

EXTERNAL COMPUTER INTERFACING

10.0 INTRODUCTION

This section discusses the 6808, 6666, and 7383 (A, B, C, and D) Recorder Boards and their respective options to interface to an external computer. Section 10.1 discusses the RS-232C Serial Interface for the 6808 and 6666 Recorder Boards. Section 10.2 discusses the general theory of operation for the four versions of the 7383 Recorder Board. Section 10.3 is an RS-232C Serial Interface Guide for the 7383B and 7383D Recorder Boards. Finally, Section 10.4 details the COROLAN Interface for the 7383A and 7383C Recorder Boards.

10.1. RS-232C SERIAL INTERFACE (6808 and 6666 only)

10.1.1 GENERAL

The RS-232C serial interface option on the 115 Fetal Monitor is designed to enable the user to interface the Model 115 to devices supporting the RS-232C standard of communication. Through this interface, the 115 supplies information such as heart rate, uterine activity, monitoring modes, event marks, and messages from either the Model 2115 or 2116 Data Entry System. This information is given in a form suitable for processing by an external computer. This interface allows knowledgeable users to develop systems capable of collecting and processing information provided by the Model 115.

10.1.2 CONTROL SIGNALS

The RS-232C Interface for the 115 is designed to make the 115 operate as a FULL DUPLEX Data Terminal (DTE); the monitor supports the following control signals:

OUTPUTS

Data Terminal Ready (DTR): This line is asserted (+12 V) whenever the 115 Fetal Monitor is on and operating. The line may be used to determine whether a 115 is powered up.

Request to Send (RTS): This line is asserted (+12 V) whenever the 115 Fetal Monitor is on and operating. The line may be used to determine whether a 115 is powered up.

Request to Send (RTS): This line is also asserted whenever the 115 is powered up.

Transmitted Data (TXD): This line provides the serial data sent by the 115.

INPUTS

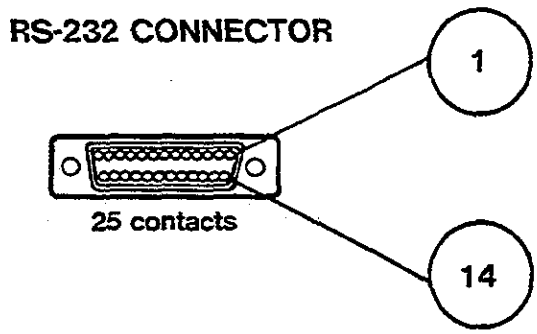
Data Set Ready (DSR): This line must be asserted in order to enable the transmission of data from the Model 115 Fetal Monitor. The line may be asserted locally by tying this line to the DTR line of the 115; it may also be connected to the DTR of the external computer (providing the external computer asserts DTR). If a modem is used, then this line would be tied to the DSR line from the modem.

Clear to Send (CTS): This line must be asserted in order to enable the transmission of data from the fetal monitor. Under conditions where no modem is used, the line can be tied to the RTS line of the fetal monitor. If a modem is used, this line should be tied to the CTS of the modem.

Received Data (RXD): This line provides the serial data sent to the 115 by an external computer.

10.1.3 DIRECT CONNECTION

Direct connection is the easiest method of connection between an external computer and the Model 115 Fetal Monitor, because it eliminates the need for modems. Interfacing to the 115 Fetal Monitor is accomplished through a 25-pin subminiature "D" (female) connector located on the rear panel. FIGURE 10-1 illustrates the connector pins.



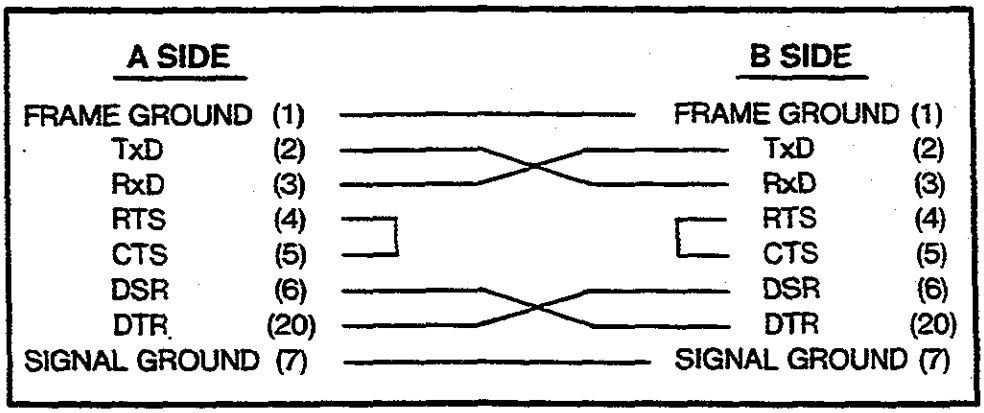
RS-232C CONNECTOR
FIGURE 10-1

The RS-232C Interface supplied with the 115 is capable of operating over varying distances depending upon the data rate used and whether the cabling is shielded or unshielded. TABLE 10-1 summarizes the maximum distances between the 115 and an external computer.

SPEED	UNSHIELDED DISTANCE	SHIELDED DISTANCE
9600 bps	250 ft.	250 ft.
4800 bps	250 ft.	1000 ft.
2400 bps	500 ft.	1000 ft.
1200 bps	3000 ft.	3000 ft.
300 bps	3000 ft.	5000 ft.

CABLE LENGTHS
TABLE 10-1

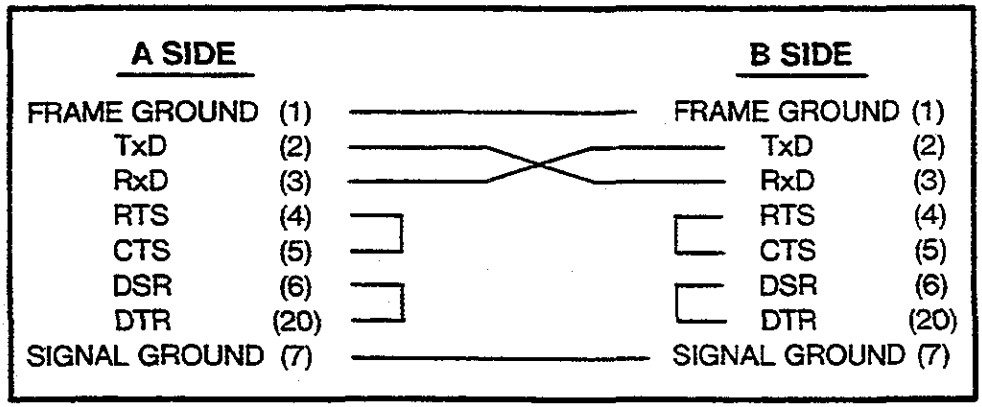
When direct connection is made to another Data Terminal Equipment (DTE), a null-modem cable is required as shown in FIGURE 10-2.



STANDARD NULL-MODEM CABLE
FIGURE 10-2

NOTE: Numbers in parentheses denote pin numbers on the RS-232C connector.

Under conditions where the DTE to which the 115 is attached does not support the DTR signal, then a special null-modem cable is required as shown in FIGURE 10-3.

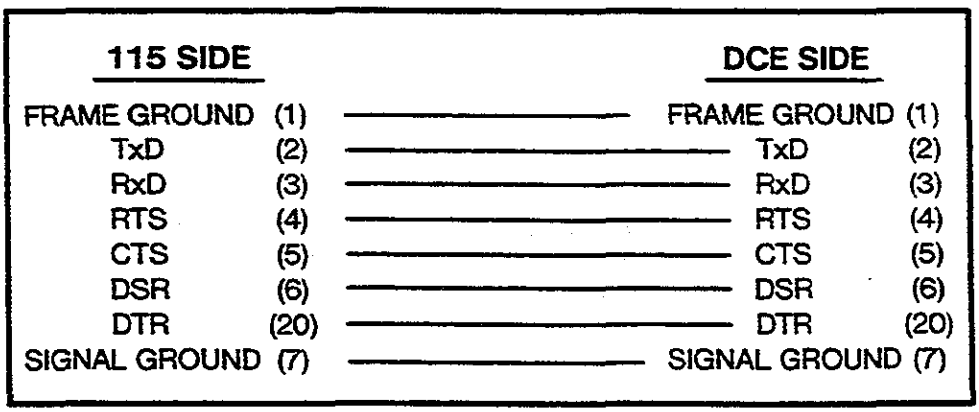


SPECIAL NULL-MODEM CABLE
FIGURE 10-3

10.1.4 INDIRECT CONNECTION

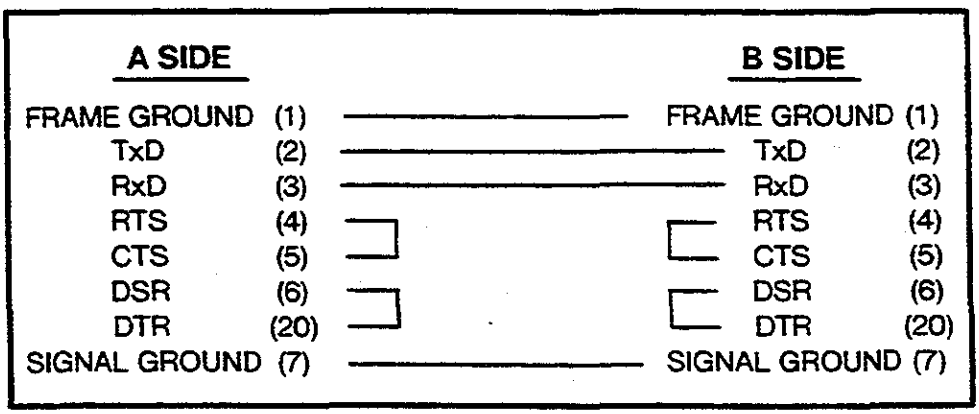
Indirect connection requires a modem. In this case the 115 Fetal Monitor requires a DCE interface cable.

Regular 115-to-DCE cabling is shown below in FIGURE 10-4.



STANDARD DCE INTERFACE CABLE
FIGURE 10-4

When interfacing the 115 to a DCE that does not have modem control lines, then the cable shown in FIGURE 10-5 is required.



SPECIAL DCE INTERFACE CABLE
FIGURE 10-5

10.1.5 USART SETUP

The data transmission rate (baud rate) for the RS-232C Interface is selected by means of a 10-position slide switch located on the left side of the Recorder Board (6808 or 6666). The baud rates available for the 115 are 9600, 4800, 2400, 1200, and 300 bits per second (bps). Each of the five rates has two positions on the switch. Adjacent to each switch is its corresponding baud rate settings.

The data format consists of 1 start bit, 8 data bits, and 2 stop bits. The 115 has 3 user-selectable parity modes. They are: no parity, odd parity, and even parity. Parity selection is made by using switches numbered 3 and 4 of the lower DIP switch package located on the right side of the Recorder Board (6808 or 6666). The positions of these switches and their functions are summarized in TABLE 10-2.

PARITY MODE	SW3	SW4
NO PARITY	ON	X*
ODD PARITY	OFF	ON
EVEN PARITY	OFF	OFF

*X denotes don't care

PARITY SELECTION
TABLE 10-2

10.1.6 UPDATE MODE

GENERAL

In the UPDATE mode, all information is transmitted from the 115 as soon as the information becomes available to the processor on the Recorder Board. Heart rate data is transmitted on a beat-to-beat basis. Uterine activity is transmitted eight times per second. Modes are transmitted during recorder startup and whenever a mode change occurs. Keypad and keyboard messages are sent as they are received. Event marks are transmitted each time a Mark button is depressed. The UPDATE mode is selected by placing switch 2 of the lower DIP switch pack in the ON position. In the UPDATE mode the 115 will not respond to any information sent from the external computer.

START-UP PROCEDURES

After power is applied to the 115, the RS-232C interface is initialized with the DTR and RTS lines asserted. The 115 will send three START OF TEXT (STX) characters (02H) to allow the external computer to synchronize itself to the 115. Due to start-up transients on the TXD line, it is possible that the external computer will not detect all three of these characters as valid. As a result, the external computer should wait until it receives the last STX character before processing any information from the 115 or before transmitting any information to the 115.

DATA FORMAT (115-TO-EXTERNAL COMPUTER)

The format of the information transmitted from the 115 is shown in FIGURE 10-6.

MONITOR TYPE	RESPONSE TYPE	MONITOR ID	DATA FIELD	END OF TEXT

TRANSMITTED DATA FORMAT
FIGURE 10-6

The definitions of the bytes are as follows:

Monitor Type: This 1-byte value indicates the type of monitor sending the information as shown below in TABLE 10-3.

Monitor	Value	ASCII Code
single-cardiotach	30H	0
dual-cardiotach	31H	1

MONITOR TYPES
TABLE 10-3

Response Type: This 1-byte value indicates the type of information being sent by the 115 as shown in TABLE 10-4.

Type	ASCII Code	Value
Heart Rate 1	\	60H
Uterine Activity	a	61H
Modes	b	62H
2115 or 2116 Modes	c	63H
Event Mark	d	64H
Heart Rate 2	e	65H

BYTE VALUES
TABLE 10-4

Monitor ID: This 1-byte value indicates the ID number of the monitor information. The value of this byte is user-selectable by the four switches of the upper DIP switch pack. The value of the byte is determined by adding the values shown in TABLE 10-5 when the switch is in the OFF position. Switches in the ON position have a value of 0.

SW#	OFF VALUE	ON VALUE
1	1	0
UPPER 2	2	0
3	4	0
4	8	0
LOWER-1	16	0

SWITCH VALUES
TABLE 10-5

Data Field: This field of n-bytes contains the actual data sent by the fetal monitor to the external computer. The contents of this field for each response is given below:

Event Mark: This field does not contain a byte whenever an event marker is pressed.

Heart Rate: Two or three ASCII BCD digits representing the value of heart rate. A value of 00 indicates a penlift condition.

Uterine Activity: Two or three ASCII BCD digits representing the value of uterine activity. A value of 128 indicates a penlift condition.

Modes: Two digits indicating mode. The first digit is the combined mode of both heart rates according to TABLE 10-6. The second digit is the mode for the uterine activity channel as listed in TABLE 10-7.

VALUE	ASCII CODE	HR1 MODE	HR2 MODE
30H	0	INOP	-
31H	1	FECG	-
32H	2	US	-
34H	4	PHONO	-
35H	5	US	MECG
36H	6	PHONO	MECG
37H	7	MECG	-
39H	9	US	FECG
3AH	:	PHONO	FECG

HEART RATE CODES
TABLE 10-6

VALUE	ASCII CODE	UA MODE
30H	0	INOP
31H	1	TOCO
32H	2	IUP
39H	9	TELEMETRY

UA CODES
TABLE 10-7

End of Text: A 1-byte field containing the value 03H.

LIMITATIONS

The only restriction on the information transmitted during the UPDATE mode occurs when then the baud rate selected is 300 bps. Under this condition, the 115 will not send any heart rate or uterine activity information. This restriction is due to the fact that at this baud rate it is impossible to transmit these parameters on a timely basis.

ERROR CONDITIONS

In the UPDATE mode, the only errors that can occur are transmission errors. These errors may be detected by the external computer as parity errors, framing errors (no valid stop bit), or invalid characters. There is no facility in the 115 to re-transmit any information found to contain an error. It is therefore up to the user to decide what action to take as a result of an error.

10.1.7 REQUEST MODE

GENERAL

In this mode the 115 will send only the information requested by the external computer. The selection of this information is done by sending a request stream to the 115. After processing the request, the 115 will then send the selected parameters to the external computer using the UPDATE mode. Therefore the information selected by the external computer will be transmitted each time the parameter changes. The requested parameters may be changed at any time by the external computer by sending a new request sequence.

DATA FORMAT

The format of the data sent by the 115 was described previously for the UPDATE MODE, however, requests transmitted to the 115 must be of the form shown in FIGURE 10-7.

MONITOR TYPE	DATA FIELD	END OF TEXT

DATA REQUEST FORMAT
FIGURE 10-7

The definitions of these bytes are as follows:

Monitor Type: This 1-byte value indicates the type of monitor the information is being sent to. 30H (ASCII 0) for single-cardiotach 115; 31H (ASCII 1) for dual-cardiotach 115.

Data Field: This 1- to 6-byte field indicates which parameters the external computer wishes to receive. The values for the bytes are given in TABLE 10-8.

VALUES	ASCII CODE	TYPE
Heart Rate 1	\	60H
Uterine Activity	a	61H
Modes	b	62H
2115 or 2116 Messages	c	63H
Event Marks	d	64H
Heart Rate 2	e	65H

DATA FIELD BYTES
TABLE 10-8

End of Text: This 1-byte field contains a 03H. If this byte is send immediately following the MONITOR ID then the 115 will cancel transmission of all data.

LIMITATIONS

As with the UPDATE MODE, this mode will not transmit heart rate or uterine activity data when the selected speed is 300 bps even if the external computer requests such information.

ERROR CONDITIONS

There are two types of errors that can occur during this mode. The first is errors that occur in data transmitted from the 115. These errors are parity errors, framing errors (no valid stop bit) or invalid characters. The second type is errors in the information transmitted to the 115. Among these errors are parity errors, framing errors, and invalid monitor ID. All of these errors cause the 115 to ignore all received data until a valid EOT (end of transmission) byte is detected. For this reason, it is suggested that the external computer re-transmit a request sequence if the 115 fails to respond properly to the request. Any invalid data during the DATA FIELD of the request is simply ignored and no error condition is set.

10.2 RECORDER BOARD THEORY OF OPERATION (7383 A, B, C, and D)

10.2.1 INTRODUCTION

The 7383 Recorder Board can replace all previous recorder boards for the Model 115 Fetal Monitor (i.e. 5808, 6709, 6808, 6665, and 6666). The four versions of this board are:

7383B: single-cardiotach w/RS-232
7383A: single-cardiotach w/COROLAN
7383D: dual-cardiotach w/RS-232
7383C: dual-cardiotach w/ COROLAN

COROLAN INTERFACE

The COROLAN interface is a coaxial cable network designed specifically to interface the Model 115 Fetal Monitor to the Corometrics MONARCH 8000 Obstetrical Management and Archival System. Through this interface the Model 115 supplies information such as heart rate and uterine activity data, monitoring modes, event marks, internal status information, and messages from either the Model 2115 or Model 2116 Data Entry System.

RS-232C INTERFACE

The RS-232C serial interface is an option allowing the user to interface the Model 115 Fetal Monitor to devices supporting the RS-232C standard of communication. Through the interface the Model 115 supplies information such as heart rate and uterine activity data, monitoring modes, event marks, and messages from either the Model 2115 or 2116 Data Entry System. This information is given in a form suitable for processing by an external computer. Knowledgeable users of RS-232C can develop systems capable of collecting and processing information provided by the Model 115 Fetal Monitor.

10.2.2 PLUGS AND CONNECTORS

The 7383 Recorder Board plugs into the card cage Motherboard. Four plugs and one miniature coaxial connector on the board itself provide the following five interfaces:

1. **P17:** This plug accepts the connector for the optional 2115 Keypad or optional 2116 Keyboard.

2. **P18:** This plug accepts the connector for the recorder stepper-motor.

3. **P19:** This plug accepts the connector for circuits performing the following six functions:

    - Thermal printhead element power (+ VHD)
    - Printhead serial-in/parallel-out shift registers and controls (DOT CLK, DOT DATA, and LOAD).
    - Printhead enable strobes $\overline{\text{STB1}}$-$\overline{\text{STB4}}$.
    - Power for PAPER LOW and PAPER OUT optosensors (OPTO DRIVE A and OPTO DRIVE B).
    - Optosensor outputs for PAPER LOW and PAPER OUT.

- Printhead electronics power (+5V).

4. **P26:** This plug accepts the connector for circuits performing one of the following two functions:

   - accepts standard signals for the RS-232C interface; or
   - accepts COROLAN LED lines and junction box device station address lines.

5. **J6:** This connector for COROLAN accepts the network data (7383 A or C only).

10.2.3 HARDWARE/SOFTWARE

BASIC FUNCTIONS

The 7383 performs the following functions:

1. Accepts message pointers, heart rate data, and uterine activity data from the Supervisor CPU Board for printing on the strip chart.

2. Accepts message pointers and patient information data entered from either the optional 2115 Keypad or the optional 2116 Keyboard. Note: Vaginal exam information must be entered in a special way when used with the MONARCH 8000 System.

3. The recorder processor builds the message string and any data string and determines the line where the string(s) will be printed. The microprocessor also contains software which calculates the graphics dot positions from the heart rate and uterine activity data.

4. Steps the recorder chart paper motor, loads the alphanumeric and graphics dot patterns into the printhead, and fires the dot elements in the printhead.

5. Formats the heart rate and uterine activity data, message data, and internal status information into a form suitable for transmission over either the COROLAN or RS-232C interface.

MICROPROCESSOR

The Microprocessor (U14) is an 8085, timed by the 6MHz oscillator on board the main CPU board. The LSB's of the address bus (A0-A7) are strobed and latched into U5. Combined with A8-A15 these lines form a complete 15-bit address bus.

MEMORY

Memory consists of a single 512K ROM (U6) and a single 8K × 8 RAM (U7). The ROM is paged into hardware (U6, pin 20) by switch pack 3 (switch 6). This eliminates the need for a separate board for each different language.

ADDRESS DECODERS

Address decoders U21, U22, and U24 select the memory or I/O peripheral device to be accessed as follows:

1. **U24:** Address lines A13-A15 select the RAM memory.

2. **U22:** Selects 1K blocks of memory for the following:

   a) recorder printhead data shift register (U32)

   b) print head control register (U31)

   c) switch 1 (SW1)

d) watchdog timer (U18)

e) 8255 peripheral interface (U14)

f) 8155 peripheral interface (U1)

g) switch 2 (SW2): for RS-232C only

h) switch 3 (SW3)

3. **U21:** Selects 16 byte blocks of I/O for the following:

a) 8530 serial communications controller (SCC) U2

b) 8237 direct memory access controller (DMA) U3

8255 (U14) PROGRAMMABLE PERIPHERAL INTERFACE

Recorder commands from the Supervisor CPU Board are sent via the unidirectional data bus (REC b) to Port A of U14. A transfer consists of a control word (8 bits) followed by a 0 to 7 word message string. Data is acknowledged through the decoding of U36.

U14 is also used to provide handshaking signals with the CPUs of both the Supervisor Board and either the optional 2115 or 2116 Data Entry System. This is managed through Port B.

PB6 of U14 is used as the LED line for the COROLAN junction box. This line also provides an error checking signal to U1. For static purposes, this line is pulsed very quickly so as not to interfere with the COROLAN LED function.

COROLAN device station addresses enter the recorder board though P26, are buffered by U46 and input to port C of U14.

8155 (U1) RAM I/O TIMER

This parallel I/O port interfaces the recorder board to the optional 2115 or 2116 Data Entry System. Keypad/keyboard data bits 0 through 4 (KBD0 - KBD4) enter the board through P17 and are sent to Port A of U1. The data is strobed using the STB line.

Keypad/keyboard control signals are buffered though U45 and sent out through P17.

The 9KHz from the card edge enters U1 where it is divided down for a 1 ms interrupt (RST 7.5) to provide the processor with the system timer.

A static environment may cause the 8155 to partially reset; to check U1 for an error condition, PC5 is output to SID of the processor (U15, pin 5). A reset will cause all outputs to revert back to inputs.

8237 (U3) DMA (DIRECT MEMORY ACCESS)

This high-performance programmable DMA controller controls transfers of data between memory and the 8530 Serial Communications Controller (U2). The 8530 sends a REQA signal to the DMA asking for service. The DMA then sends a HREQ (hold request) signal to the processor requesting bus mastership. The CPU responds with a HLDA (hold acknowledge) signal; this active high signal indicates the CPU has relinquished control of the system buses. At this point, the DMA takes control of the system's address and data buses. Data is then either a) read from the 8530 and written to main memory, or b) read from main memory and written to the 8530. This transfer of data is done by the block transfer method. There is continuous operation until the entire block of data is transferred. At the end of each block, bus mastership is returned to the processor.

SWITCH SETTINGS

There are 3 8-position slide switches on the 7383 Recorder Board which control the options for the following:

- RS-232C Device Station ID
- RS-232C Mode (Update or Request)
- Parity for RS-232C
- RS-232C Baud Rate
- Monitor Type (English, German . . .)
- Interface (COROLAN or RS-232C)
- Chart Speed
- Heart Rate Scale

The switch settings, listed in TABLES 10-9 A, B, and C, are defined by:

0 = ON, and **1 = OFF**

SWITCH NUMBERS	SETTINGS	OPTION
1 2 3 4 5	User Selectable	Monitor Device ID
6	0	RS-232C Request Mode
	1	RS-232C Update Mode
7	0	No Parity for RS-232C
	1	Parity for RS-232C
8	0	Odd Parity for RS-232C
	1	Even Parity for RS-232C

SWITCH PACK 1
TABLE 10-9A

SWITCH NUMBERS	SETTING	OPTION
1 2 3	0 0 0	9600 bps RS-232C Baud Rate
	1 0 0	4800 bps RS-232C Baud Rate
	0 1 0	2400 bps RS-232C Baud Rate
	1 1 0	1200 bps RS-232C Baud Rate
	0 0 1	300 bps RS-232C Baud Rate

SWITCH PACK 2
TABLE 10-9B

SWITCH NUMBERS	SETTING	OPTION	
		single-cardiotach	dual-cardiotach
1 2 3	0 0 0	English	English
	1 0 0	French*	French
	0 1 0	German*	German
	1 1 0		Spanish
	0 0 1	Japanese	Japanese
4 5	0 0	No External Interface	
	1 0	RS-232C Interface	
	0 1	COROLAN Interface	
	1 1	Undefined	
6	0	2 cm/min Chart Paper Speed	
	1	3 cm/min Chart Paper Speed	
7	0	30-240 BPM Heart Rate Scale	
	1	50-210 BPM Heart Rate Scale	

*only valid for 50-210 BPM scale chart paper

SWITCH PACK 3
TABLE 10-9C

10.2.4 PRINTING FUNCTIONS

PAPER-LOW/PAPER-OUT DETECTION

Reflection of the DRIVE A LED from chart paper causes optosensor A to conduct holding PAPER LOW low. Black squares near end of chart result in insufficient reflection and PAPER LOW (U8, pin 10) goes high. This drives pin 13 of the dual comparator U8 low which controls I/O port PB6 (U1, pin 35).

Similarly, reflection of the DRIVE B LED from chart paper causes optosensor B to conduct holding PAPER OUT low. If paper runs out, reflection from black roller is insufficient and PAPER OUT (U8, pin 5) goes high. This drives pin 2 of the dual comparator U8 low which controls I/O port PB5 (U1, pin 34).

Due to variations of optosensors, R47 and R52, are used to adjust the threshold voltages for optosensor B and optosensor A, respectively.

STEPPER-MOTOR CIRCUIT

The stepper motor circuit is comprised of driver U17 (SAA1027) and level shifter U8. This circuit provides the timing of all the windings and sources the necessary power. To step the motor, PB2 of U14 is toggled from low to high and back to low again. This is performed by writing 20H and then 0H to set and reset pin 20 of U14.

The motor is stepped via level shifter U8 and driver U17. The trigger pulse which can be seen at TP1 causes the motor to take one step. The required pulse is a 10 μs active high signal. Specifications on frequency are a function of the chart speed as shown in TABLE 10-10.

CHART SPEED	STEPPING ADVANCE
1 cm/min	133 ms
3 cm/min	44 ms
25 cm/min (paper advance)	5 ms

STEPPING TIMES
TABLE 10-10

The processor then proceeds to the printing routine.

10.3 RS-232C SERIAL INTERFACE (7383 B AND D ONLY)

10.3.1 GENERAL

To enable the RS-232C Interface of the 7383 Recorder Board, ensure switch SW3-4 is OFF and SW3-5 is ON. The information in this section is not meant to provide a complete understanding of the RS-232C standard of serial communication. It is provided as additional information for knowledgeable users.

Electronics Industries Association (EIA) defines RS-232C voltage levels as follows:

- Logic 1 is represented by a negative voltage between −3 V and −25 V.
- Logic 0 is represented by a positive voltage between +3 V and +25 V.

10.3.2 CONTROL SIGNALS

The RS-232C Interface for the 115 is designed to make the 115 operate as a FULL DUPLEX Data Terminal (DTE); the monitor supports the following control signals:

OUTPUTS

Data Terminal Ready (DTR): This line is asserted (+ 12 V) whenever the 115 Fetal Monitor is on and operating. The line may be used to determine whether a 115 is powered up.

Request to Send (RTS): This line is also asserted whenever the 115 is powered up.

Transmitted Data (TXD): This line provides the serial data sent by the 115.

INPUTS

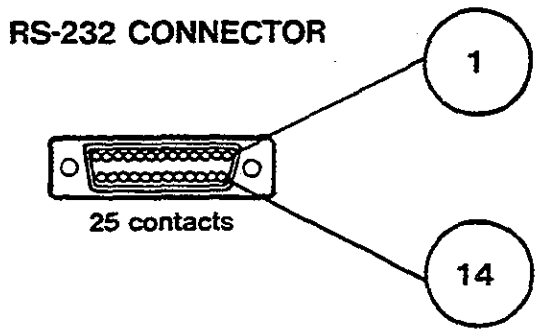
Data Set Ready (DSR): This line must be asserted in order to enable the transmission of data from the Model 115 Fetal Monitor. The line may be asserted locally by tying this line to the DTR line of the 115; it may also be connected to the DTR of the external computer (providing the external computer asserts DTR). If a modem is used, then this line would be tied to the DSR line from the modem.

Clear to Send (CTS): This line must also be asserted in order to enable the transmission of data from the fetal monitor. Under conditions where no modem is used, the line can be tied to the RTS of the fetal monitor. If a modem is used, this line should be tied to the CTS of the modem.

Received Data (RXD): This line provides the serial data sent to the 115 by an external computer.

10.3.3 DIRECT CONNECTION

Direct connection is the easiest method of connection between an external computer and the Model 115 Fetal Monitor, because it eliminates the need for modems. Interfacing to the 115 Fetal Monitor is accomplished through a 25-pin subminiature "D" (female) connector located on the rear panel. FIGURE 10-8 defines the connector pins:



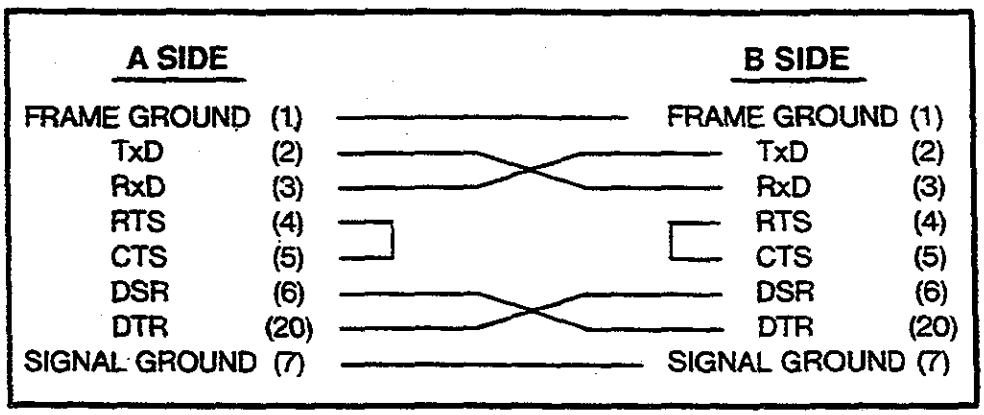
RS-232C CONNECTOR
FIGURE 10-8

The RS-232C Interface supplied with the 115 is capable of operating over varying distances depending upon the data rate used and whether the cabling is shielded or unshielded. TABLE 10-11 summarizes the maximum distances between the 115 and an external computer:

SPEED	UNSHIELDED DISTANCE	SHIELDED DISTANCE
9600	250 ft.	250 ft.
4800	250 ft.	1000 ft.
2400	500 ft.	1000 ft.
1200	3000 ft.	3000 ft.
300	3000 ft.	5000 ft.

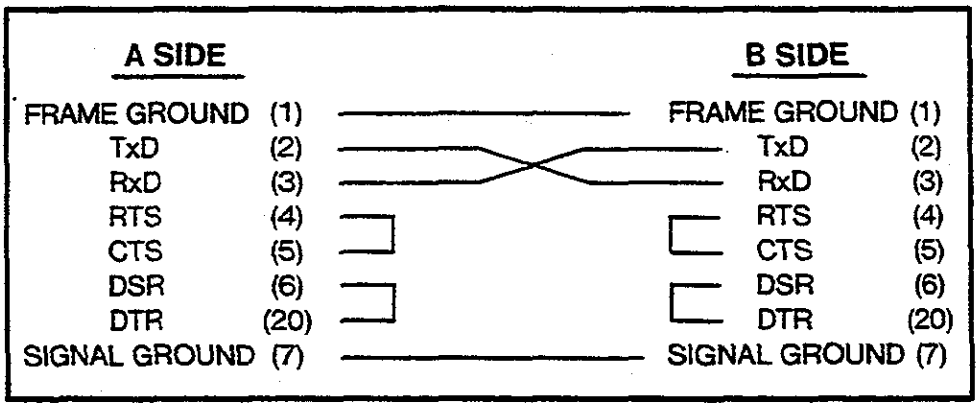
CABLE LENGTHS
TABLE 10-11

When direct connection is to another Data Terminal Equipment (DTE), a null-modem cable is required as shown in FIGURE 10-9.



STANDARD NULL-MODEM CABLE
FIGURE 10-9

Under conditions where the DTE to which the 115 is attached does not support the DTR signal, then a special null-modem cable is required as shown in FIGURE 10-10.

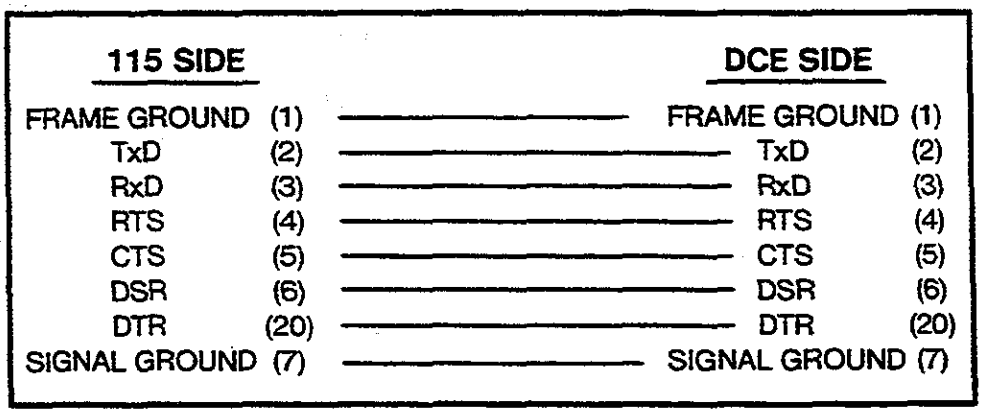


SPECIAL NULL-MODEM CABLE
FIGURE 10-10.

10.3.4 INDIRECT CONNECTION

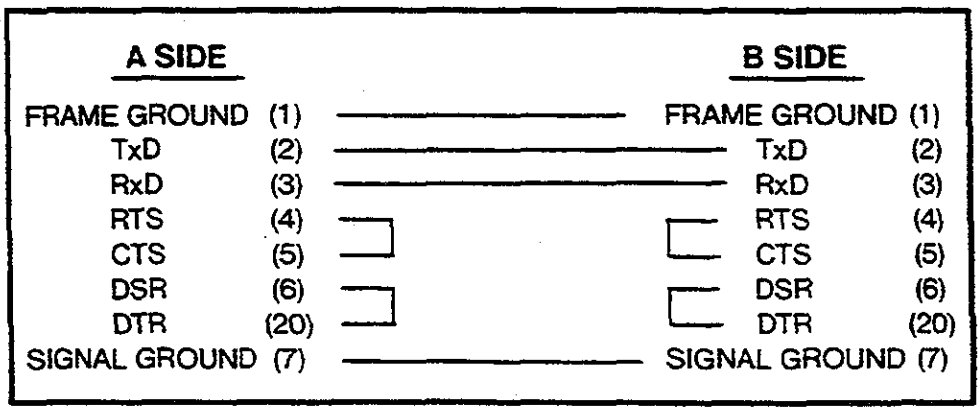
Indirect connection requires a modem. In this case the 115 Fetal Monitor requires a DCE interface cable.

Regular 115-to-DCE cabling is shown in FIGURE 10-11.



STANDARD DCE INTERFACE CABLE
FIGURE 10-11

When interfacing the 115 to a DCE that does not have modem control lines, then the cable shown in FIGURE 10-12 is required:



SPECIAL DCE INTERFACE CABLE
FIGURE 10-12

10.3.5 HARDWARE/SOFTWARE

8530 (2) SERIAL COMMUNICATIONS CONTROLLER

The 8530 (U2) is the serial communication controller (SCC) interface performing the following primary functions:

- Converts 8-bit parallel data on the CPU data bus to a serial bit stream which is conveyed to the TXDB port (pin 25) consisting of 8 serial data bits (LSB) first, one or zero parity bits, 1 start bit, and two stop bits.
- Converts an 8-bit serial data stream from the RXDB port (pin 27) to 8 parallel bits in the form specified by SW1 (switches 7 and 8).
- Sets the RS-232C baud rate as determined by SW2 (switches 1, 2, and 3) for both transmit and receive.
- Detects framing and overrun errors (and parity errors if parity-error detection is enabled).
- Generates and accepts RS-232C signals used in modem control and similar applications (DTR, RTS, DSR, and CTS).

SCC INITIALIZATION AND CONTROL

The baud rate for transmission is selected by means of an 8-position slide switch located on the Recorder Board. The baud rates available for transmission and the corresponding switch settings are listed in TABLE 10-12.

BAUD RATE (bits per second)	SW2-1	SW2-2	SW2-3
9600	ON	ON	ON
4800	OFF	ON	ON
2400	ON	OFF	ON
1200	OFF	OFF	ON
300	ON	ON	OFF

BAUD RATE SWITCHES
TABLE 10-12

RS-232C DATA FORMAT

The data format consists of 1 start bit, 8 data bits, and two stop bits. The monitor has three user-selectable parity modes which are selected by an 8-position slide switch SW1. The parity modes and the corresponding switch settings are shown in TABLE 10-13.

PARITY MODE	SW1-7	SW1-8
NO PARITY	ON	X*
ODD PARITY	OFF	ON
EVEN PARITY	OFF	OFF

*X = don't care

PARITY SELECTION
TABLE 10-13

10.3.6 UPDATE MODE

GENERAL

To enter the UPDATE Mode, ensure switch SW1-6 is OFF.

START-UP PROCEDURES

After power is applied, the RS-232C interface is initialized with the DTR and RTS lines asserted high. Three START OF TEXT (STX) characters (02H) allow the external computer to synchronize itself to the fetal monitor. Due to start-up transients on the TXD line, it is possible that the external computer will not detect all three of these characters as valid. As a result, the external computer should wait until it receives the last STX character before processing any information from the 115 or before transmitting any information to the 115.

DATA FORMAT (115-TO-EXTERNAL COMPUTER)

The format of the information transmitted from the 115 is shown in FIGURE 10-13

MONITOR TYPE	RESPONSE TYPE	MONITOR ID	DATA FIELD	END OF TEXT

TRANSMITTED DATA FORMAT
FIGURE 10-13

Monitor Type: This 1-byte value indicates the type of monitor sending the information as shown in TABLE 10-14.

Monitor	Value	ASCII Code
single-cardiotach	30H	0
dual-cardiotach	31H	1

MONITOR TYPES
TABLE 10-14

Response Type: This 1-byte value indicates the type of information being sent by the 115 as shown in TABLE 10-15.

Type	ASCII Code	Value
Heart Rate 1	\	60H
Uterine Activity	a	61H
Modes	b	62H
2115 or 2116 Messages	c	63H
Event Mark	d	64H
Heart Rate 2	e	65H

BYTE VALUES
TABLE 10-15

Monitor ID: This 1-byte value indicates the ID number of the monitor information. The value of this byte is user-selectable using switches 1 through 5 of switch pack SW1. The value of the byte is determined by adding the values shown in TABLE 10-16.

SW1-#	OFF VALUE	ON VALUE
1	1	0
2	2	0
3	4	0
4	8	0
5	12	0

SWITCH VALUES
TABLE 10-16

Data Field

This field of n-bytes contains the actual data sent by the fetal monitor to the external computer. The contents of this field for each response is given below:

Event Mark: This field does not contain a byte whenever an event marker is pressed.

Heart Rate: Two or three ASCII BCD digits representing the value of heart rate. A value of 00 indicates a penlift condition.

Uterine Activity: Two or three ASCII BCD digits representing the value of uterine activity. A value of 128 indicates a penlift condition.

Modes: Two digits indicating mode. The first digit is the combined mode of both heart rates according to TABLE 10-17. The second digit is the mode for the uterine activity channel as listed in TABLE 10-18.

VALUE	ASCII CODE	HR1 MODE	HR2 MODE
30H	0	INOP	
31H	1	FECG	
32H	2	US	
34H	4	PHONO	
35H	5	US	MECG
36H	6	PHONO	MECG
37H	7	MECG	
39H	9	US	FECG
3AH	:	PHONO	FECG

HEART RATE CODES
TABLE 10-17

VALUE	ASCII CODE	UA MODE
30H	0	INOP
31H	1	TOCO
32H	2	IUP
39H	9	TELEMETRY

UA CODES
TABLE 10-18

End of Text: A 1-byte field containing the value 03H.

LIMITATIONS

The only restriction on the information transmitted during the UPDATE mode occurs when the baud rate selected is 300 bps. Under this condition, the 115 will not send any heart rate or uterine activity information. This restriction is due to the fact that at this baud rate it is impossible to transmit these parameters on a timely basis.

ERROR CONDITIONS

In the UPDATE mode, the only errors that can occur are transmission errors. These errors may be detected by the external computer as parity errors, framing errors (no valid stop bit), or invalid characters. There is no facility in the 115 to re-transmit any information found to contain an error. It is therefore up to the user to decide what action to take as a result of an error.

10.3.7 REQUEST MODE

GENERAL

To operate in the REQUEST Mode, SW1-6 must be set to the ON position. In this mode the 115 will send only the information requested by an external computer. The selection of this information is done by sending a request stream to the 115. After processing the request, the 115 will then send the selected parameters to the external computer using the UPDATE mode. Therefore, the information selected by the external computer will be transmitted each time the parameter changes. The requested parameters may be changed at any time by the external computer by sending a new request sequence.

DATA FORMAT

The format of the data sent by the 115 was described previously for the UPDATE MODE, however, requests transmitted to the 115 must be of the form shown in FIGURE 10-14.

MONITOR TYPE	DATA FIELD	END OF TEXT

DATA REQUEST FORMAT
FIGURE 10-14

The definitions of these bytes are as follows:

Monitor Type

This 1-byte value indicates the type of monitor information is being sent to. 30H (ASCII 0) for 115 without dual-cardiotach; 31H (ASCII 1) for 115 with dual-cardiotach.

Data Field

This 1- to 6-byte field indicates which parameters the external computer wishes to receive. The values for the bytes are given in TABLE 10-19.

VALUES	ASCII CODE	TYPE
60H	\	Heart Rate 1
61H	a	Uterine Activity
62H	b	Modes
63H	c	2115/2116 Messages
64H	d	Event Marks
65H	e	Heart Rate 2

DATA FIELD BYTES
TABLE 10-19

End of Text

This 1-byte field contains a 03H. If this byte is sent immediately following the MONITOR ID then 115 will cancel transmission of all data.

LIMITATION

As with the UPDATE mode, this mode will not transmit heart rate or uterine activity when the selected speed is 300 bps even if the external computer requests such information.

ERROR CONDITIONS

There are two types of errors that can occur during this mode. The first is errors that occur in data transmitted from the 115. These errors are parity errors, framing errors (no valid stop bit), or invalid characters. The second type is errors in the information transmitted to the 115. Among these errors are parity errors, framing errors, and invalid monitor ID. All of these errors cause the 115 to ignore all received data until a valid EOT (end of transmission) byte is detected. For this reason, it is suggested that the external computer re-transmit a request sequence if the 115 fails to respond properly to the request. Any invalid data during the DATA FIELD of the request is simply ignored and no error condition is set.

10.4 COROLAN COMMUNICATION

10.4.1 GENERAL

To enable the COROLAN Interface of the 7383 Recorder Boards, ensure switch SW3-4 is ON and SW3-5 is OFF.

The COROLAN network employs a subset of the synchronous data link control (SDLC) protocol for serial data communication. This local area network (LAN) solves the earlier RS-232C problems of speed and installation complexities.

The structure of the COROLAN network is based on the International Standard Organization (ISO) open system interconnect model, however, COROLAN is not compatible with other LANs. The newtwork provides communication between up to 33 devices with one acting as the primary and all others acting as secondaries. All communication between devices is initiated and controlled by the primary. Communication is accomplished by the primary polling each secondary and each secondary in turn responding with the appropriate status or data. In this case, the Model 801 computer acts as the primary device, while each fetal monitor acts as a secondary device.

All data and control information is converted to a serial stream prior to transmission across COROLAN. Likewise all data and control information received from COROLAN must be converted from a serial stream back into parallel form.

10.4.2 COROLAN/SDLC STRUCTURE

The transmission of information over the COROLAN network closely adheres to the IBM SDLC standard. This bit-oriented protocol defines a frame sequence (or packet description) as the form shown in FIGURE 10-15.

Preamble	Flags	Address	Control	I Field	CRC	Flags	Illegal Manchester Code

FRAME SEQUENCE
FIGURE 10-13

PREAMBLE

The preamble is a function of the 7960 (U20). During data transmission, the 7960 inserts a 32-bit preamble. During data reception, the 7960 strips off the 32-bit preamble. This preamble insertion/deletion corresponds to Mode 0 of the 7960. This 32-bit preamble consists of a Manchester 1 followed by 30 bits of alternating Manchester code. The last bit is a Manchester 1.

FLAG

At the beginning of packet data this identifies a start of frame condition. At the end, this identifies the end of frame condition. Packet data is placed between two flags.

ADDRESS

The address byte is always the address of the secondary device. When a packet is sent from the primary device to a secondary device, the device station address alerts the device of the information. If a packet is sent from a secondary device to the primary device, the address informs the primary which device has sent the packet. The address is the device station wallplate address.

CONTROL

The control field indicates the type of information contained in a packet's information field (I-field).

INFORMATION FIELD

All data is sent in this field. This proprietary information contains codes representing the following:

- Monitor Type (vendor)
- Monitor Options (language, speed, scale, reset status, buffer status)
- Monitor Modes (HR modes, UA mode)
- Data

CRC FIELD

These 2 bytes are the result of a cyclic redundance check. A computation is done on the A, C, and I fields at the transmitting end, checking if errors have been introduced between transmission and reception.

ILLEGAL MANCHESTER CODE

This end of message signals the end of transmission. The logic level is held high for two entire bit periods.

MANCHESTER ENCODING

The 7960 encodes the serial data into Manchester serial data defined by the following:

- Logic levels are represented by the direction of transition at the midpoint of a bit.
- Logic "1" is represented by a low-to-high transition.
- Logic "0" is represented by a high-to-low transition.
- Transitions between bits occur if necessary to establish proper logic transition for the next bit.

Refer to FIGURE 10-16.

MANCHESTER CODE
FIGURE 10-16

10.4.3 NETWORK DATA RECEPTION

Manchester encoded data enters the 7383 Recorder Board through miniature coaxial cable connector J6 where it is sent to transformer T1. This data is then decoded to SDLC (Synchronous Data Link Control) packet data by U20 (Am7960) and sent to the SCC (Serial Communications Controller) chip U2 (Am8530). The SCC removes flag characters and checks for the device station address for this monitor. The address is from the device station junction box entering the board at U14, Port C. If the correct address is received, U2, pin 10 (REQA) will go low requesting U3, Direct Memory Access Controller, to place a byte in memory. When U3 receives a byte, pin 10 (HRQ) goes low requesting control of the bus from the processor (U15). When the processor completes its current instruction, U15, pin 38 (HLDA) is activated granting the bus mastership. After the DMA (U3) places the byte in memory, U2, pin 10, goes high until the next byte is received. The process is repeated until all of the bytes in a packet have been received.

A full 15-bit address bus is formed by U3, similar to the processor, by latching the upper 8 bits by U4. Read, write, and I/O Port functions remain the same as if the processor were controlling the bus and accessing the memory.

10.4.4 NETWORK DATA TRANSMISSION

If the recorder board is polled and information is ready to be sent, the transmission of data is initiated by setting control port (U31, pin 6) and setting U2, pin 17 (RTS line). This sets the transmission of the carrier only; the carrier can be located at transformer T1, provided the line is free from activity. This is done by SCC (U20) which gates off transmission by the activity detect line (pin 10).

After a short time, U2, pin 10 (REQA) goes low requesting data transmission from the DMA (U3). When the DMA (U3) receives the request for data transmission, U3, pin 10 (HRQ) goes low requesting bus mastership from the processor. When the processor finishes its current instruction, pin 38 (HLDA) is activated granting bus mastership. The DMA (U3) then reads the appropriate data from memory and writes it to the SCC (U2). This process is repeated until all the bytes in the packet data have been written to the SCC (U2). The SCC (U2) will interrupt the processor informing of the completed packet transmission. The processor then turns off control port (U31, pin 6), and in turn the SCC RTS line cuts off carrier transmission.

10.4.5 ERROR DETECTION

If the primary device (computer) receives an error from a secondary device (monitor or 810 Interface), such as a CRC error, the primary device will re-transmit a request for information. The primary will re-try up to 5 times.

If the secondary device receives an error from the primary, the secondary will respond on the next poll with a frame reject message.

10.4.6 HARDWARE/SOFTWARE

8530 (U2) SERIAL COMMUNICATIONS CONTROLLER

The 8530 (U2) is the serial communications controller (SCC) interface performing the following primary functions:

- Converts 8-bit parallel data on the CPU data bus to serial bit stream which is conveyed to the TXDA port (pin 15) in SDLC format.
- Converts an 8-bit stream of serial data from the RXDA port (pin 13) to 8 parallel bits.
- Removes flags (sync characters) and looks for the device station address of the secondary station.
- Is programmed (Address Search Mode Bit = 1) to receive only those frames whose address matches WR6.
- Adds flags to packets sent from the DMA and/or processor. Adds CRC at the end.
- Detects framing and overrun errors (zero insertion and abort conditions). This causes the DMA to ignore the data.

7960 (U20) MANCHESTER CONTROLLER CHIP

This coded data transceiver performs the following primary functions:

- Detects line activity.
- During reception, decodes Manchester encoded packet data, strips off 32-bit preamble (mode 0), encodes in SDLC, and sends to 8530.
- During transmission, accepts SDLC packet data from 8530, adds 32-bit preamble (mode 0), and encodes in Manchester format packet data.
- Drives isolation transformer T1; the receiver and transmitter are connected in parallel to operate as a half duplex system.